REMARKS

35 U.S.C. 112 Rejections

Claims 1 and 3-60 are rejected under 35 U.S.C. 112, first paragraph as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, has possession of the claimed invention. The Examiner states "the instant specification teaches post growth cooling and annealing at less than 625°C in Fig 3; however there is no positive recitation that heating to a higher third temperature occurs." Applicants respectfully submit that the Examiner is incorrect. Applicants describe the cool down process of step 36 of Fig. 3 at page 6, line 22 to page 7 line 2. "The cool-down process begins at a temperature above 700°C" (see page 6 line 22) and ends at "room temperature" (see page 6 line 29). The summary also states that the cool-down process takes place "starting above 700°C and ending at room temperature." See page 4, line 7. The next step in Fig. 3 after cool-down is step 38, which is described at page 7 lines 17-20:

> In step 38 of Fig. 3, a post-growth anneal is performed on the wafer to remove essentially all of the H within the p-type layers. This anneal, in one embodiment is below 625°C. Temperatures as low as 100°C are expected to work, although temperatures in the range of 400-625°C are believed to be best.

Since the cool-down may take the device down to room temperature, and in some embodiments, the anneal after cool-down takes raises the temperature to greater than 100°C, the application specifically teaches "after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C" as recited in claims 1 and 31.

Claims 4 and 34 are rejected under 35 U.S.C. 112, first paragraph, as being based on a disclosure which is not enabling. Specifically, the Examiner states "the instant specification teaches forming an n-type semiconductor layer cap and removing the cap layer prior to annealing the p-type layer, the step of removing the cap layer is critical or essential to the

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practice of the invention, but not included in the claim(s) is not enabled by the disclosure." Applicants note at page 9 line 2 that the "n-type cap is then removed (step 44) by a conventional etching step . . . ." Emphasis added.

Applicants respectfully point out that the examiner has not met his burden for establishing an enablement rejection. MPEP 2164.04 states:

> In order to make a rejection, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention.
>
> . . . .
>
> The language [of the rejection] should focus on those factors, reasons, and evidence that lead the examiner to conclude that the specification fails to teach how to make and use the claimed invention without undue experimentation, or that the scope of any enablement provided to one skilled in the art is not commensurate with the scope of protection sought by the claims. This can be done by making specific findings of fact, supported by the evidence, and then drawing conclusions based on these findings of fact . . . . [S]pecific technical reasons are always required." (Emphasis in original omitted, emphasis added.)

The Examiner's rejection is totally lacking any specific technical reasons, findings of fact, or evidence required by the above-quoted section of the MPEP. In order to reject claims 4 and 34 for lack of enablement, the Examiner must provide evidence or technical reasons disputing Applicants' assertion that removal of the cap layer is conventional. Since the Examiner has failed to provide such evidence or reasons, the Examiner has not formulated a proper enablement rejection.

Applicants respectfully submit that removal of the cap layer is sufficiently described to allow a person of skill in the art to practice the invention without undue experimentation. On page 9 line 8, Applicants teach chemical etching and plasma etching may be used on III-nitride layers. In addition, Applicants attach a page from *High Brightness Light Emitting Diodes* edited by Stringfellow and Craford and published in 1997, demonstrating that it was known prior to the filing date of the present application to a person of skill in the art to use reactive ion etching to etch III-nitride layers. Finally, Applicants note that U.S. Patent No. 5,926,726 to Bour et al., which is presumed to be enabled and issued prior to the filing date of

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the present application, teaches at column 9 lines 5-6 that "n-type GaN cap layer may be removed by etching," without further any further teaching of how to etch. Applicants respectfully submit that Applicants own specification, as well as Applicant's evidence of what was known to a person of skill in the art prior to Applicants' filing date, demonstrate that claims 4 and 34 are enabled.

In view of the above arguments, Applicants respectfully request that the Examiner withdraw his rejections under 35 U.S.C. 112, first paragraph.

35 U.S.C. 103 Rejections

Claims 1, 3-5, 12-35, and 42-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour et al., U.S. Patent No. 5,926,726 (hereinafter "Bour") in view of Koike et al., U.S. Patent No. 5,811,319 (hereinafter "Koike") and Furukawa et al., U.S. Patent 6,017,807 (hereinafter "Furukawa"). Applicants respectfully traverse the rejection because Bour specifically teaches away from combination with Furukawa.

Claims 1 and 31 recite "growing in a chamber a III-V nitride compound semiconductor layer at a first temperature . . . cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process . . . and after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C."

The Examiner states:

> Bour et al also does not teach heating said p-type layer to a third temperature greater than the second temperature and less than 625°C.
>
> In a method of forming a P-type GaN compound, note entire reference, Furukawa et al teaches after a p-type gallium nitride compound semiconductor layers formed by chemical vapor deposition, the p-type gallium nitride layers are thermally annealed at more than 400°C and the p-type impurity can be more effectively activated so that p-type gallium nitride compound semiconductor layers which have fewer crystal defects and lower resistivity can be formed (abstract, col 4, ln 5-67 and col 6, ln 35-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Bour et al with Furukawa et al annealing at a

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temperature greater than 400°C to form a semiconductor layer which has fewer defects and lower resistivity.

It would not have been obvious to modify Bour's process to add an anneal after cool-down is complete, as taught by Furukawa, because Bour specifically teaches that it is undesirable to complete cool-down prior to performing an anneal. See, for example, column 3, lines 46-50 of Bour which list problems associated with such a post-cool-down anneal including high processing costs, and potential contamination from exposure to the atmosphere accompanying ex-situ processing. Even if the post-cool-down anneal is performed in situ, a person of skill in the art would still expect to encounter high processing times and costs and potential contamination, and would therefore not be motivated to modify Bour's process.

MPEP section 2141 teaches "When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to: . . . The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination." Bour's entire teaching is devoted to providing a process that avoids the use of a post-cool-down anneal, and thus cannot possibly suggest the desirability of combining Bour with a reference that uses a post-cool-down anneal. Since Bour specifically teaches away from providing a post-cool-down anneal, Bour cannot be combined with any reference that teaches such an anneal, including Furukawa. Koike is cited as teaching a particular hole density and adds nothing to the deficiencies of Bour and Furukawa described above.

Applicants respectfully submit that claims 1 and 31 distinguish over Bour, Furukawa, and Koike because Bour and Furukawa cannot be combined as proposed by the Examiner. Claims 1 and 31 are therefore allowable. Claims 3-5 and 12-30 depend from claim 1 and are therefore allowable for at least the same reason. Claims 32-35 and 42-60 depend from claim 31 and are therefore allowable for at least the same reason.

Claims 6, 9, 11, 36, 39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour, Furukawa, and Koike as applied to claims 1, 3-5, 12-35, and 42-60,

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further in view of Takatani, U.S. Patent No. 6,100,174. Claims 6, 9, and 11 depend from claim 1 and are therefore allowable for at least the reasons stated above for claim 1. Claims 36, 39, and 41 depend from claim 31 and are therefore allowable for at least the reasons stated above for claim 31. Takakani adds nothing to the deficiencies of Bour, Furukawa, and Koike with respect to claims 1 and 31. Accordingly, claims 6, 9, 11, 36, 39, and 41 are allowable over the combination of Bour, Furukawa, Koike, and Takatani.

Claims 10 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour, Furukawa, Koike, and Takatani, as applied to claims 6, 9, 11, 36, 39, and 41, and further in view of Peng et al., U.S. Patent No. 5,895,223. Claim 10 depends from claim 9, which depends from claim 1. Claim 10 is therefore allowable for at least the reasons stated above for claim 1. Claim 50 depends from claim 31 and is therefore allowable for at least the reasons stated above for claim 31. Takakani and Peng et al. add nothing to the deficiencies of Bour, Furukawa, and Koike with respect to claims 1 and 31. Accordingly, claims 10 and 50 are allowable over the combination of Bour, Furukawa, Koike, Takatani, and Peng et al.

Claims 13 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour, Furukawa, and Koike as applied to claims 1, 3-5, 12-35, and 42-60, further in view of Peng et al. Claim 13 depends from claim 5, which depends from claim 1. Claim 13 is therefore allowable for at least the reasons stated above for claim 1. Claim 43 depends from claim 35, which depends from claim 31. Claim 43 is therefore allowable for at least the reasons stated above for claim 31. Peng et al. adds nothing to the deficiencies of Bour, Furukawa, and Koike with respect to claims 1 and 31. Accordingly, claims 13 and 43 are allowable over the combination of Bour, Furukawa, Koike, and Peng et al.

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Claims 7, 8, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour, Furukawa, and Koike as applied to claims 1, 3-5, 12-35, and 42-60, further in view of Nitta et al., U.S. Patent No. 5,789,265. Claims 7 and 8 depend from claim 5, which depends

from claim 1. Claims 7 and 8 are therefore allowable for at least the reasons stated above for claim 1. Claims 37 and 38 depend from claim 35, which depends from claim 31. Claims 37 and 38 are therefore allowable for at least the reasons stated above for claim 31. Nitta et al. adds nothing to the deficiencies of Bour, Furukawa, and Koike with respect to claims 1 and 31. Accordingly, claims 7, 8, 37, and 38 are allowable over the combination of Bour, Furukawa, Koike, and Nitta et al.

In view of the above arguments, Applicants respectfully request allowance of all pending claims. Should the Examiner have any questions, the Examiner is invited to call the undersigned at (408) 382-0480.

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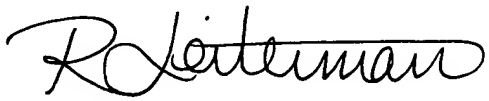
Respectfully submitted,



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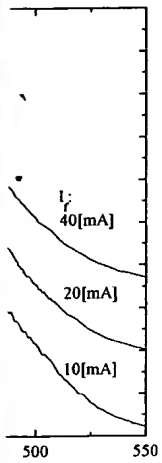

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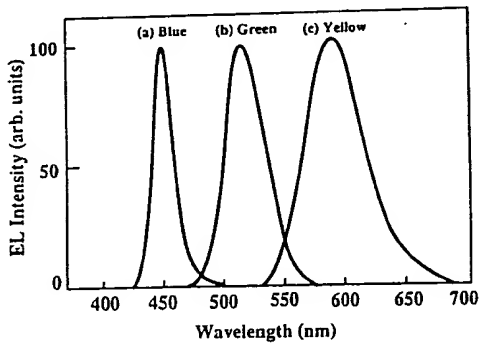

FIG. 28. Electroluminescence (EL) spectrum of a light-emitting diode having a very thin $Ga_{1-x}In_xN$ active layer $0.12 < x < 0.7$). (Reprinted from Nakamura *et al.*, 1995b, *Jpn. J. Appl. Phys.* **34**, L797, with the permission of the publisher.)

2. ELECTRODE

Sapphire had been the most widely used substrate for epitaxial growth. This has required a special design for the electrical contacts to both the n-type and acceptor-doped layers. The nitride researchers in the 1970s made an n-type electrode on the side of the n-type layer. The electrode for the acceptor doped layer was formed on top of the film. Indium and Al were used as the electrodes for the n-type and acceptor-doped layers, respectively.

Ohki *et al.* (1981) used highly conducting polycrystalline n-type GaN grown by HVPE for the n-type electrode. Patterned silicon dioxide (SiO_2) was used to grow polycrystalline GaN. By using this technique, the electrodes for the n-type GaN can be formed more easily on the top surface. This has enabled fabrication of a flip-chip–type LED.

Koide *et al.* (1991) first used the reactive ion etching technique to etch the p-type layer, thus allowing formation of the n-type electrode on top of the etched surface. A chlorine-containing compound, such as boron chloride (BCl_3), is commonly used for the etchant gas.

Edmond *et al.* (1996) fabricated bright blue LEDs consisting of a Zn-doped GaInN active layer on a 6H-SiC substrate. The 6H-SiC is itself conducting, therefore, the n-type electrode can be formed on the rear surface of the 6H-SiC substrate. A shorting ring is used to reduce the effect of the nitride–SiC energy barrier.

Today, Al or Ti–Al is mostly used to form ohmic contact to n-type GaN (Foresi and Moustakas, 1993). Specific resistivities as low as $10^{-7}\,\Omega\cdot cm^2$ have been achieved. Titanium forms nitride compounds such as titanium nitride (TiN), which are metallic. This enables the formation of even more superior low-resistance contacts.